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J Gateley, M Blatt, D Chen, S Cooke, P Desai, M ... - Proceedings of the Design Automation Conference (DAC), 1995 - portal.acm.org

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The design and implementation of an extendible instruction-set simulator

P Zadarnowski, U Thesis - BE thesis, School of Computer Science and Engineering, ..., 2000 - cse.unsw.edu.au

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IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language

IS Board - 1995 - ieeexplore.ieee.org

... and supported verification **simulation**, timing analysis, fault **simulation**, and test ... **Miriam Blatt** James Brandt Dennis B. Brophy Randal E. Bryant John A. Busco ...

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Gate-level power and current simulation of CMOS integrated circuits

A Bogliolo, L Benini, G De Micheli, B Ricco - IEEE TRANS VERY LARGE SCALE INTEGR VLSI SYST, 1997 - ieeexplore.ieee.org

... 2. Peak current versus overall power consumption of ... Data are obtained by electrical-level simulation. ... Gate Model When evaluating the **average** power consumption ...

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Clock skew optimization for peak current reduction

L Benini, P Vuillod, A Bogliolo, G De Micheli - Journal of VLSI Signal Processing, 1997 - springerlink.com

... approx- imation of the **average** current profile. ... to the combinational logic from simulation of our ... effective optimization algorithm for **peak** current minimization ...

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Modelling utility-scale wind power plants. Part 1: Economics

MR Milligan - Wind Energy, 1999 - doi.wiley.com

... of the other units with probabilistic simulation algorithm ... This **average** cost can, at the modeller's option, include ... capacity on-peak for the off-peak target to ...

Cited by 7 - Web Search - nrel.gov - dlnet.vt.edu - adsabs.harvard.edu

Study of power consumption for high-performance reconfigurable computing architectures

BF Veale, N Lopez-Benitez - 1999 - students.ou.edu

... This approach requires the simulation of time-domain data ... over the entire interval corresponding to the input data ... fourth clock cycle, on average, and a value ...

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book Logic synthesis for low power VLSI designs

S Iman, M Pedram - 1998 - print.google.com

... 8.4.3 Functional simulation to speed up optimization ... In these applications **average** power consumption is a ... In this context, **peak** power (maximum possible power ...

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LA Lev, A Charnas, M Tremblay, AR Dalal, BA ... - IEEE J. Solid-State Circuits, 1995 - ieeexplore.ieee.org
... Member, IEEE, Chakra R. Srivatsa, Member, ZEEE, **David Greenhill**, ... during a fetch,
saving power and reducing ... A. **Simulation** Corners and Speedup Ratios Large CPU ...
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Initial results on the performance and cost of vector microprocessors

CG Lee, DJ DeVries - PROC ANNU INT SYMP MICROARCHITECTURE. pp. 171-182. 1997 - portal.acm.org

... One possible reason for the lack of results could be that, in addition to the usual
simulation tools, a significant amount of compiler infrastructure is also ...

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F Klass, C Amir, A Das, K Aingaran, C Truong, R ... - IEEE JOURNAL OF SOLID-STATE CIRCUITS, 1999 - ieeexplore.ieee.org

... Klass, Chaim Amir, Ashutosh Das, **Kathirgamar Aingaran**, Cindy Truong ... induced by the input, output, power supply, and ... 3), a simulation was performed in which the ...

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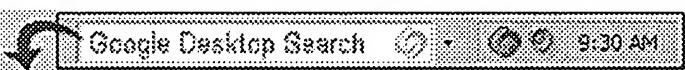
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